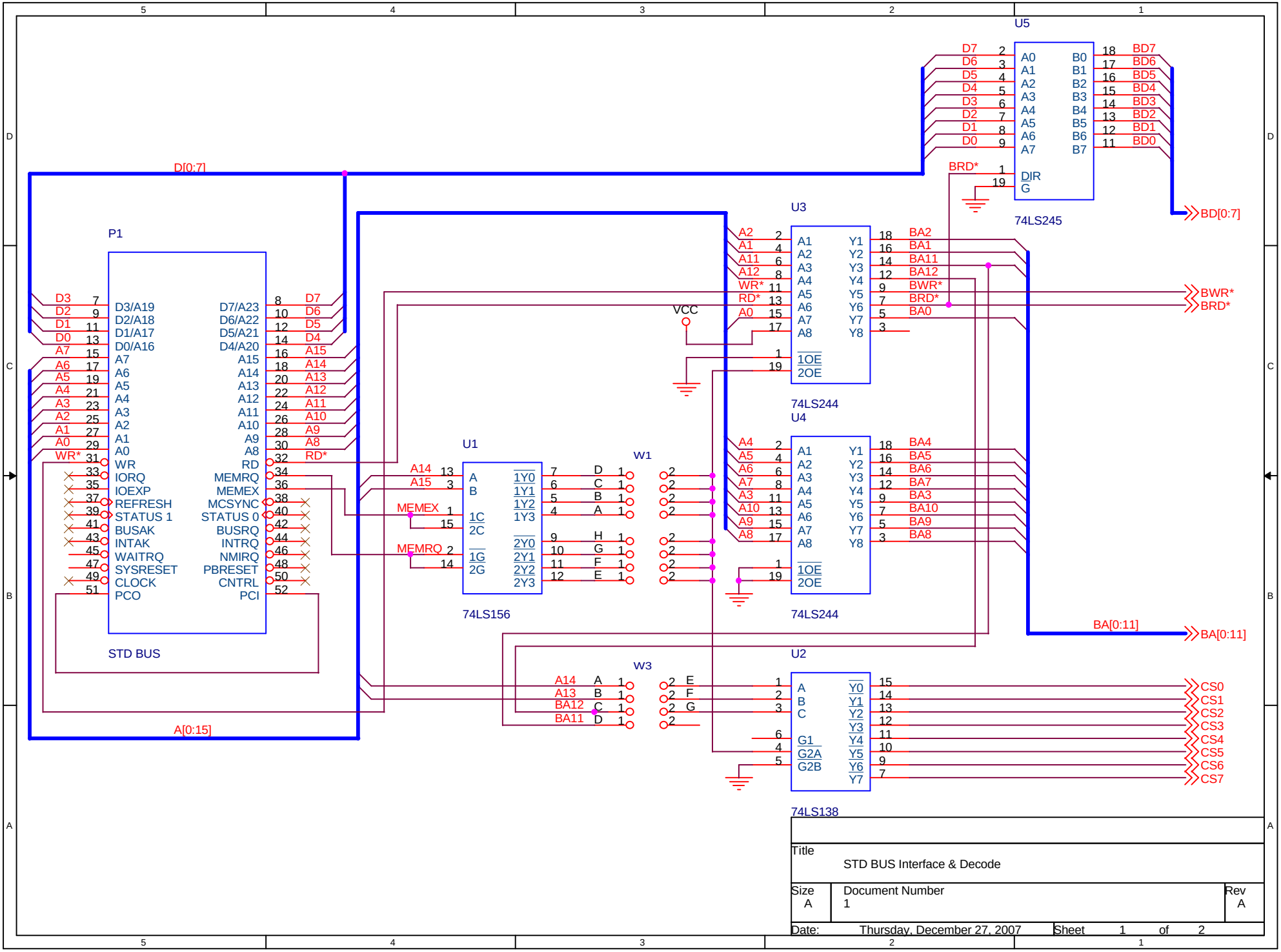
U5
74LS245
D[0:7]
BD[0:7]
BRD*
P1
STD BUS
D3/A19
D2/A18
D1/A17
D0/A16
A7
A6
A5
A4
A3
A2
A1
A0
WR
IORQ
IOEXP
REFRESH
STATUS 1
BUSAK
INTAK
WAITRQ
SYSRESET
CLOCK
PCO
D7/A23
D6/A22
D5/A21
D4/A20
A15
A14
A13
A12
A11
A10
A9
A8
RD
MEMRQ
MEMEX
MCSYNC
STATUS 0
BUSRQ
INTRQ
NMIRQ
PBRESET
CNTRL
PCI
A[0:15]
U3
74LS244
U4
74LS244
VCC
BWR*
BRD*
BA[0:11]
U1
74LS156
W1
W3
U2
74LS138
CS0
CS1
CS2
CS3
CS4
CS5
CS6
CS7
Title
STD BUS Interface & Decode
Size
A
Document Number
1
Rev
A
Date: Thursday, December 27, 2007
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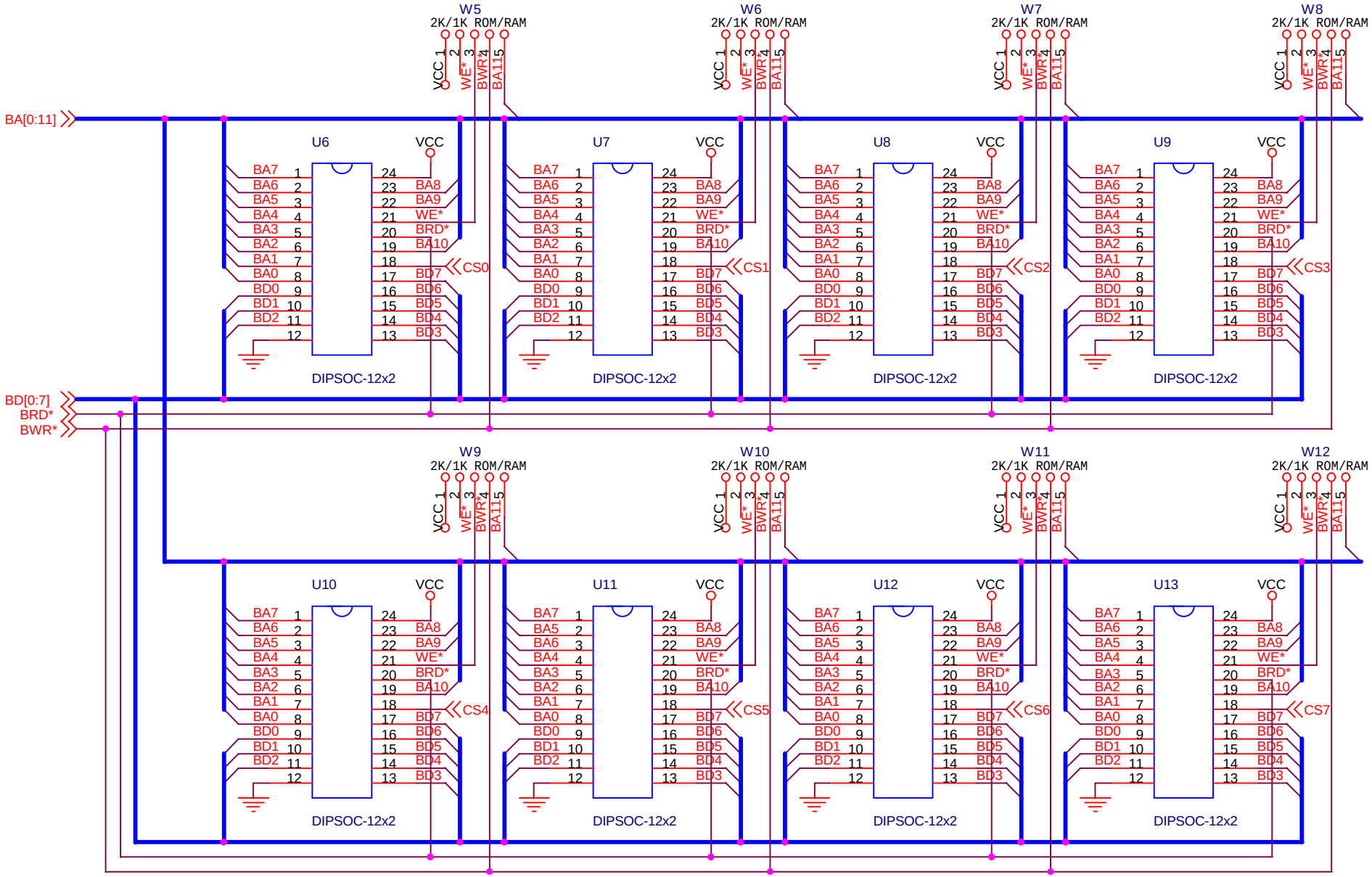

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