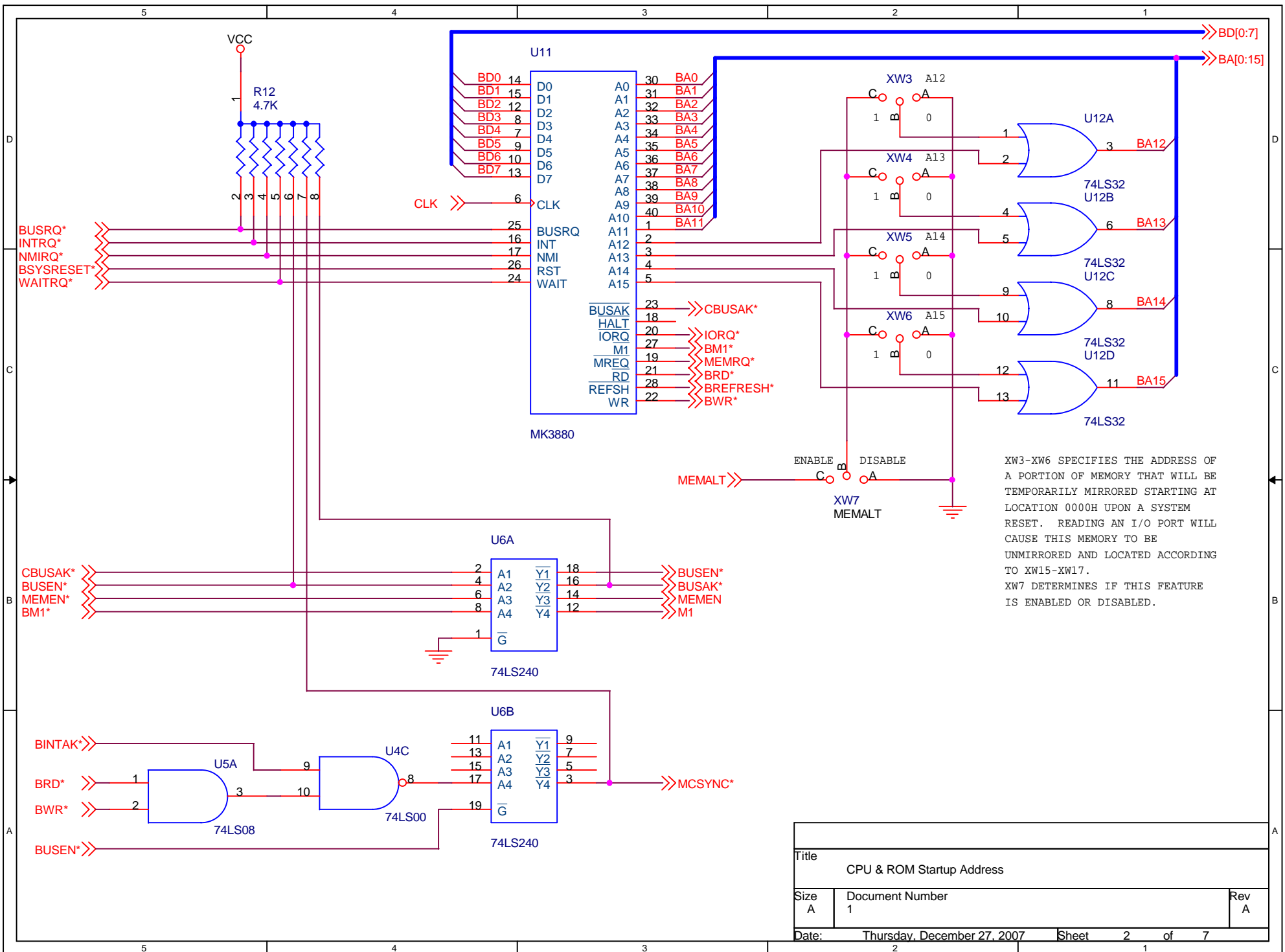


Title		
STD Bus Interface		
Size	Document Number	Rev
A	1	A
Date:	Thursday, December 27, 2007	Sheet 1 of 7



XW3-XW6 SPECIFIES THE ADDRESS OF A PORTION OF MEMORY THAT WILL BE TEMPORARILY MIRRORED STARTING AT LOCATION 0000H UPON A SYSTEM RESET. READING AN I/O PORT WILL CAUSE THIS MEMORY TO BE UNMIRRORED AND LOCATED ACCORDING TO XW15-XW17. XW7 DETERMINES IF THIS FEATURE IS ENABLED OR DISABLED.

Title		
CPU & ROM Startup Address		
Size	Document Number	Rev
A	1	A
Date:	Thursday, December 27, 2007	Sheet 2 of 7
	2	1

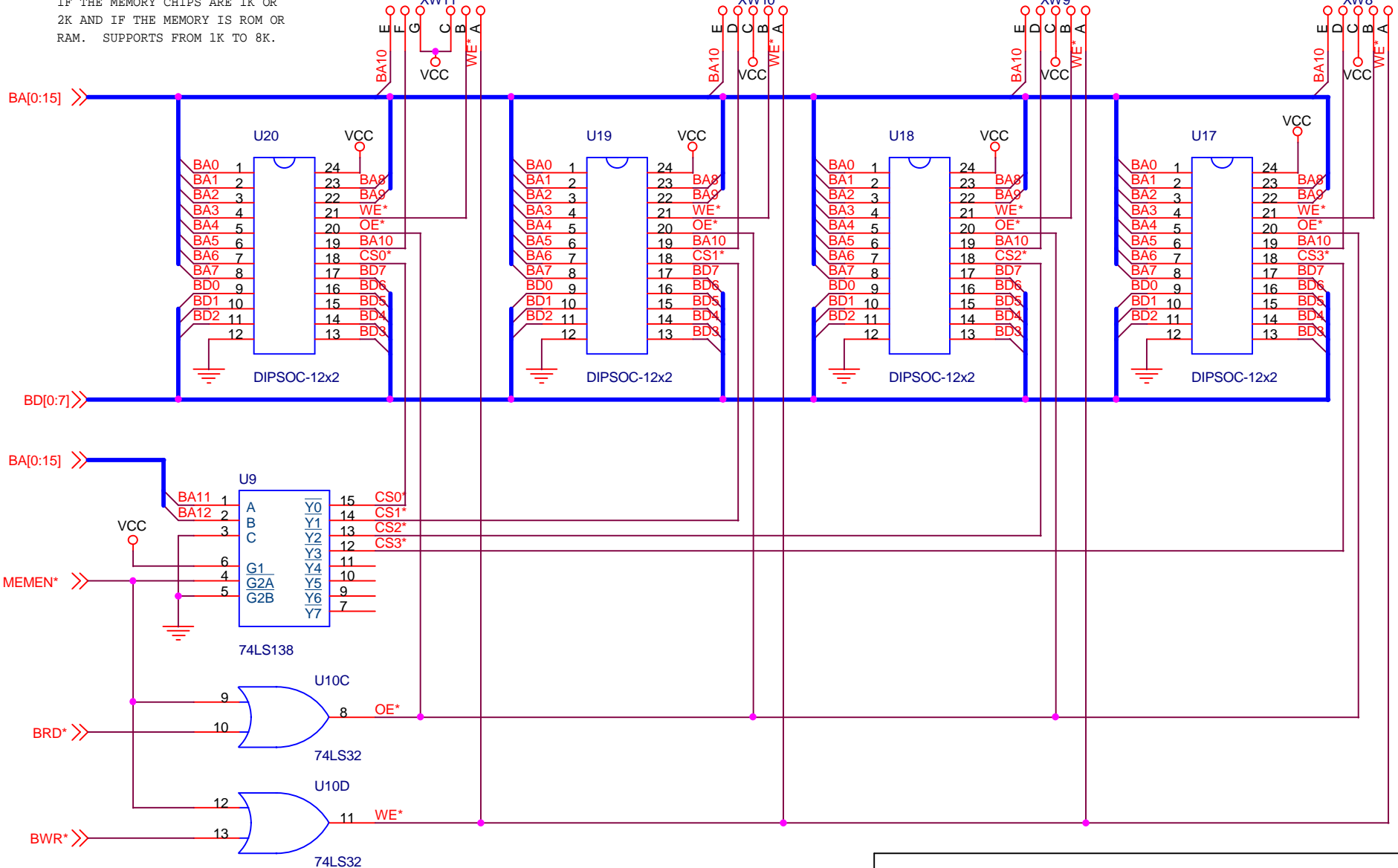
XW8, XW9, XW10 & XW11 DETERMINE IF THE MEMORY CHIPS ARE 1K OR 2K AND IF THE MEMORY IS ROM OR RAM. SUPPORTS FROM 1K TO 8K.

2K/1K ROM/RAM

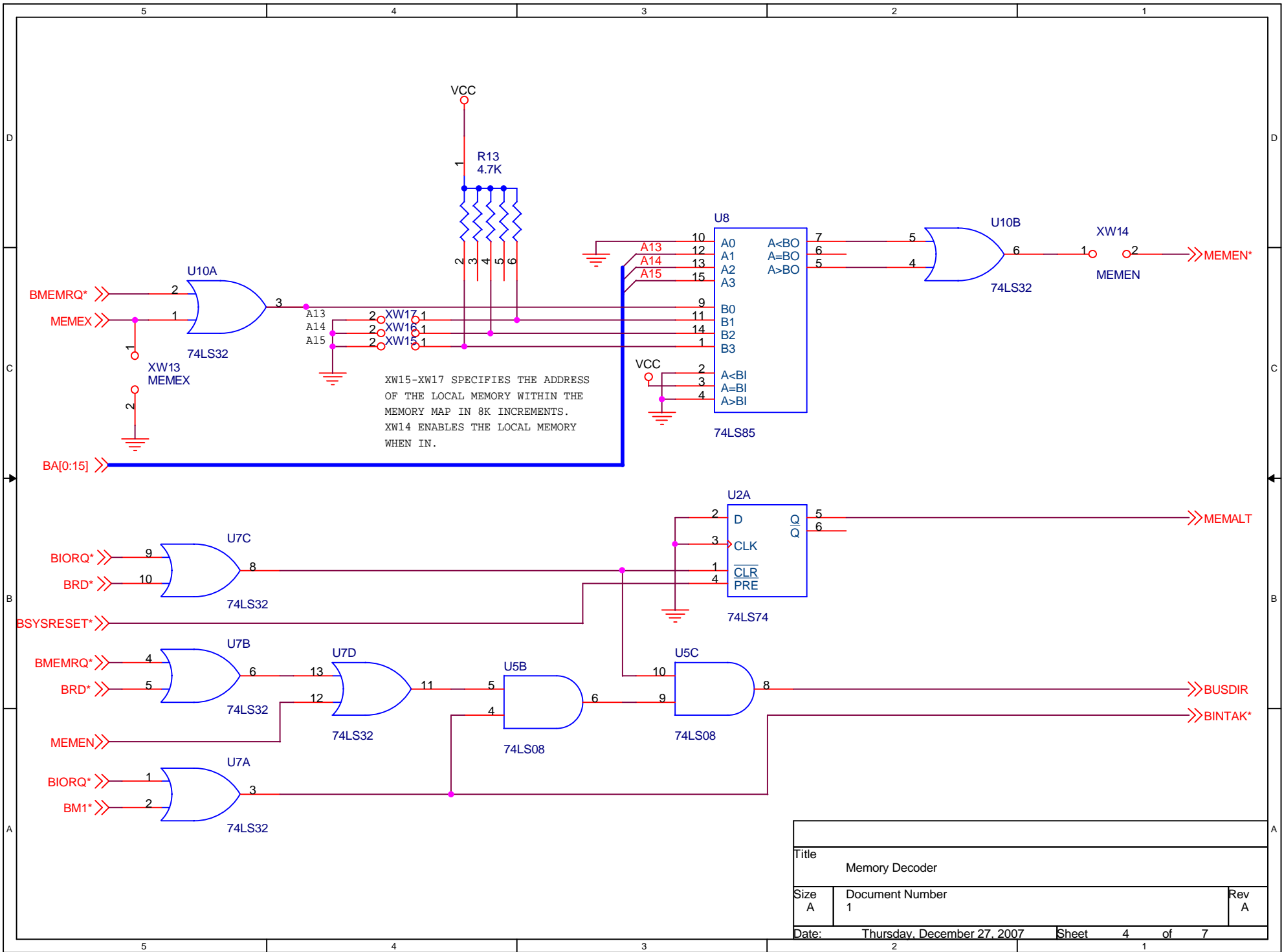
2K/1K ROM/RAM

2K/1K ROM/RAM

A 2K/1K ROM/RAM

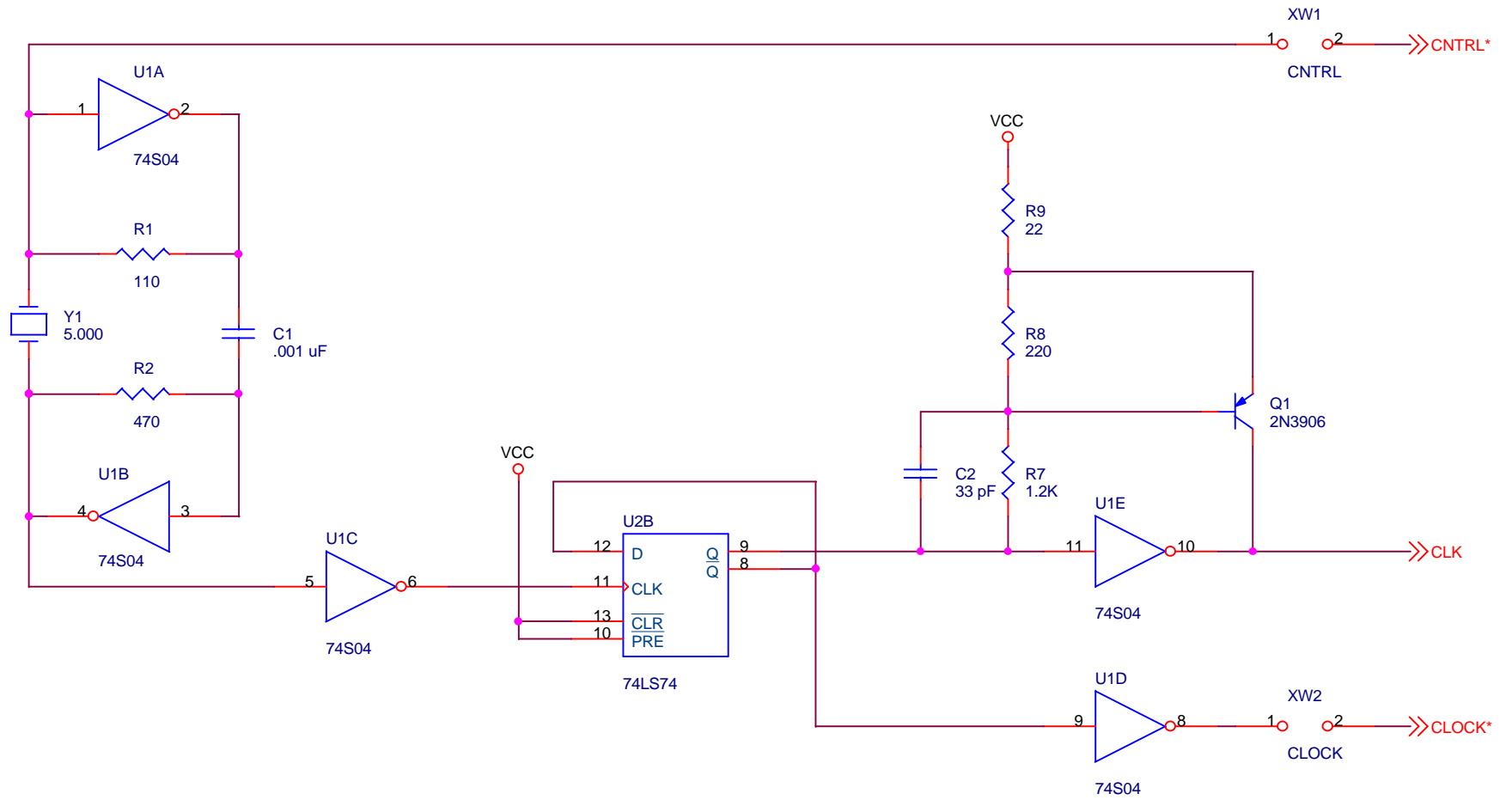


Title		
Local Memory		
Size	Document Number	Rev
A	1	A
Date: Thursday, December 27, 2007		
Sheet		3 of 7
2		1

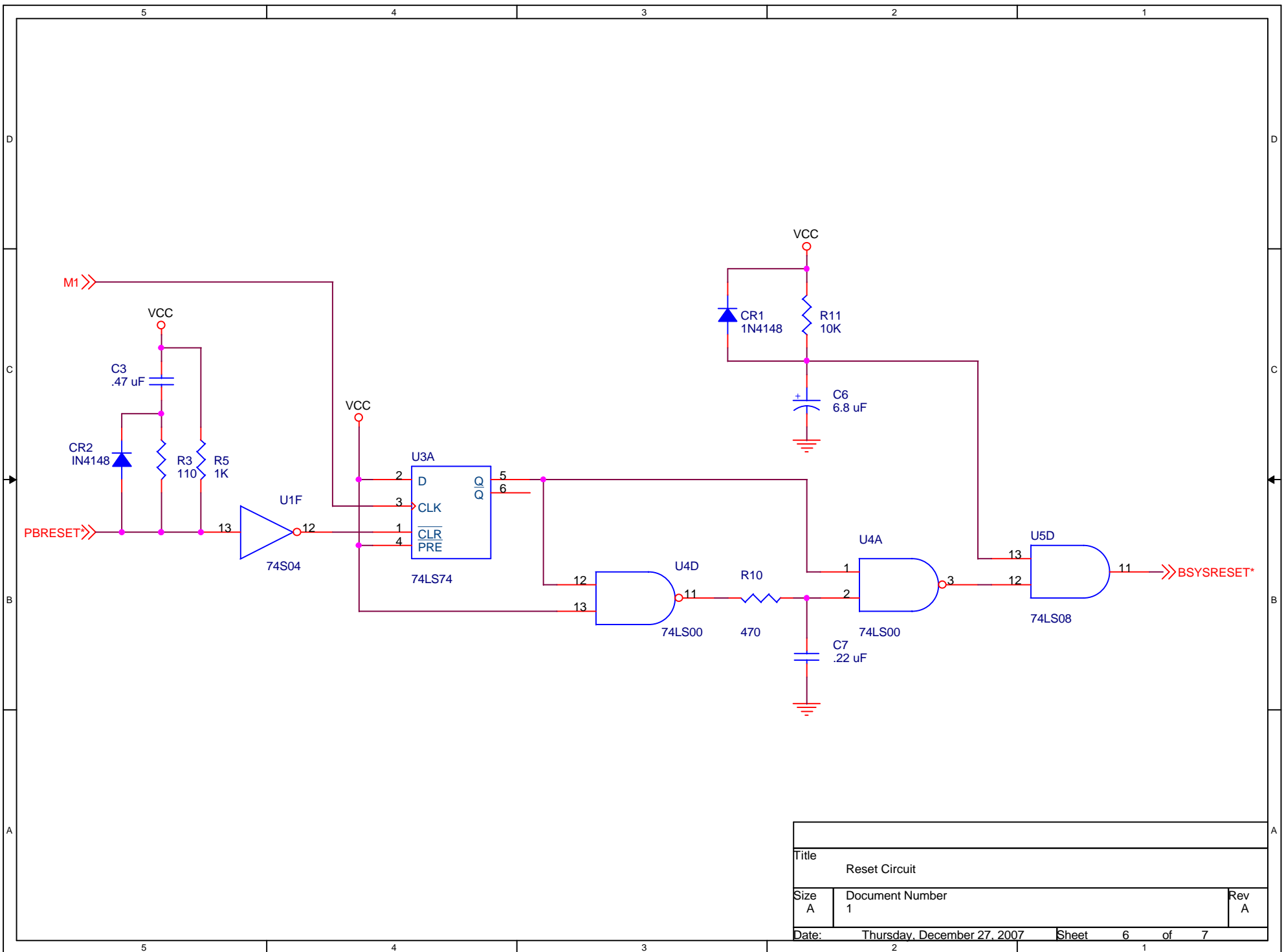


XW15-XW17 SPECIFIES THE ADDRESS OF THE LOCAL MEMORY WITHIN THE MEMORY MAP IN 8K INCREMENTS. XW14 ENABLES THE LOCAL MEMORY WHEN IN.

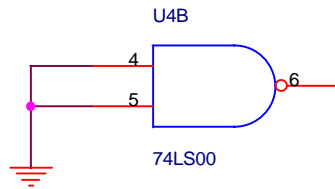
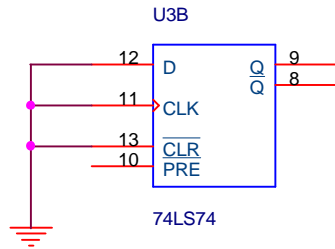
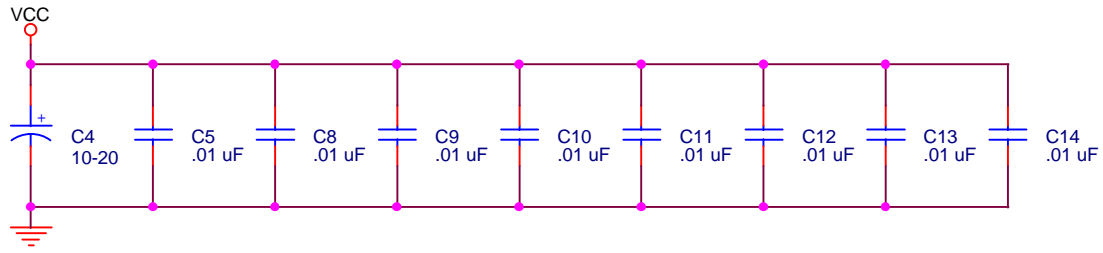
Title Memory Decoder		
Size A	Document Number 1	Rev A
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Title		
System Clock		
Size	Document Number	Rev
A	1	A
Date:	Thursday, December 27, 2007	Sheet 5 of 7
	2	1



Title		
Reset Circuit		
Size	Document Number	Rev
A	1	A
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	2	1



Title		
Miscellaneous		
Size	Document Number	Rev
A	1	A
Date:	Thursday, December 27, 2007	Sheet 7 of 7
	2	1